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David J. Allstot

The integration of photodetectors with IC circuits provides a significant improvement over conventional designs. Featuring noise reduction, extended frequency responses, lower power consumption, and data operations, these integrated devices open challenging opportunities for many applications. One type of photodetector has the potential for important applications in the life science and remote sensing fields — a photodetecting device that detects modulated light while rejecting ambient light. A circuit that can reject very bright ambient light yet provide high AC gain for the best signal-to-noise ratio was simulated, constructed and tested by discrete components, and excellent results were obtained. Using 80 klux tungsten light, this device detected an 0.08 lux light signal modulated at 16 kHz, rejecting more than 120 dB of DC light. This circuit was demonstrated by application to a plant physiology study, and the results were also significant. Based on a 1.2 μm n-well CMOS process, a monolithic device that rejects DC light was designed and simulated by using HSPICE and the SWITCAP2 programs. It was found that a rejection of about 112 dB of DC light may be realized by the CMOS monolithic device. A structure extending this sensor to an imaging device that rejects DC ambient light is also proposed.

A Photodetecting Device That Rejects Ambient Light

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Major Professor, representing Electrical & Computer Engineering

Redacted for Privacy

Chair of Department of Electrical & Computer Engineering

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Chapter1. Introduction

1.1 System Introduction

The integration of IC circuits and photodetectors provides the possibility of having a single chip that is capable of extended analog and digital operations. As stated in the above abstract, more and more photodetectors and imaging devices are being engineered to achieve improved performance and unique functions, such as noise reduction, extended frequency responses, low power consumption, and data processing with feature extraction.

By applying NMOS technology to the manufacturing of self-scanning linear photodiode arrays, Hamamatsu has been able to supply higher performance and increased flexibility for photometric instrument manufacturers. Application of these arrays have been simplified because of low power consumption [1]. The monolithic combination of photodiode and transimpedance amplifiers on a single chip eliminates the problems commonly encountered in discrete designs, such as leakage current errors, noise pickup, and gain peaking due to stray capacitances [2].

In the field of fiber optic receiver designing, Chaiki Takano and other researchers developed an optical receiver block that worked at a speed of 5 Gb/s for applications, such as board-to-board or chip-to-chip data communications [3]. The optical receiver with a metal-semiconductor-metal photodetector and 0.35 μm gate junction FET's was monolithically integrated on a GaAs substrate. As an example of low noise application, a

GaAs transimpedance preamplifier for fiber-optic receivers was designed and fabricated with two gain stages and an inductor-FET load structure [4].

CMOS circuits are also commonly used to extend the performance of photodetecting devices. In 1985, Allstot and others [5] implemented a 27-channel CMOS photodetector array. In this design, a bootstrapping technique provided the DC voltage shift necessary to interface the photodiode with a Widlar stage, which significantly improved the frequency response by reducing the effective capacitance of the photodiode. N- and P-channel Widlar mirrors were alternated in a cascading configuration to obtain a large overall compression factor and maintain a wide bandwidth.

By introducing digital integrated circuits into imaging devices, Erik and others introduced a novel, high speed smart camera MAPP2200 [6]. The programmable sensor, commercially available since 1991, has structures that combine a 256×256 photodiode array with a linear array of 256 A/D converters and 256 bit-serial processing elements on one chip. Each processing element has an 8-bit A/D register, 96 bits of memory, and an ALU connected on a 1-bit bus [7]. With some algorithms to the programmable sensor, a line frequency of 15-20 kHz has been realized, which is considerably faster than that used by other methods.

Some applications require the measurement of a weak signal in the presence of strong ambient light. For example, in remote sensing sciences it is extremely desirable to detect a weak modulated signal in the presence of ambient light, such as sun light. Sometimes a dark room can be prepared, or optical filters can be used to block the unwanted background light; but if the measuring light is modulated, then the DC background light can be electronically removed. Simple capacitive coupling at an amplified output may be adequate, however, large feedback resistors or bright ambient

light may cause the amplifier to saturate. A circuit that can reject very bright ambient light, yet provide high AC gain for the best signal-to-noise ratio, is well known [8, 9]. The circuit uses two amplifiers, one for signal amplification and the other for DC rejection.

1.2 Thesis Outline

As a result of this work, a photodetecting device that rejects DC light was analyzed and constructed, and a CMOS monolithic IC realization was proposed and simulated. Chapter 2 will give a detailed description of the system and the analysis of the circuit. Chapter 3 will present the performance of the special device implemented from discrete components, and will demonstrate one application of the circuit to plant physiology study. Chapter 4 will describe the design steps of the circuits, including the internal op amp design and the switched-capacitor integrator. Finally, the HSPICE and SWITCAP2 simulation results will be presented and a structure of an imaging device that rejects DC ambient light will be discussed. Chapter 5 will summarize the work.

Chapter 2. Circuit Analysis Of A Photodetecting Device That Rejects DC Light

The photodetecting device, shown in figure 2.1, consists of a transimpedance amplifier, and a non-inverting integrator which provide a DC cancellation current to the transimpedance amplifier through the resistor R3. The current flowing through R3 cancels the DC current from the photodiode at the signal frequencies below the pole frequency of the integrator to drive the output of the transimpedance amplifier to 0 V.

2.1 Circuit Analysis

The special detector was constructed by discrete components and tested, but the design originated with circuit analysis. Figure 2.1 gives an overview of the circuit. The op amp below and the feedback resistor R4 form a conventional transimpedance amplifier. The op amp on the top, resistors R1, R2, and capacitors C1 and C2 form a non-inverting integrator. The matching pole of the integrator, set by R1 and C1, prevents the high-pass filter from passing signals above the pole frequency feeding directly back into the summing junction of the transimpedance amplifier.

By applying KCL to the nodes 2, 7 and 8, the following equations can be written:

Node 2: $$\frac{(0-V_{out})}{R_4}+\frac{(0-V_9)}{R_3}=I_D$$ ---------- (1)

Node 7: $$\frac{V_7-0}{R_2}+\frac{(V_7-V_9)}{1/(S\cdot C_2)}=0$$ ---------- (2)

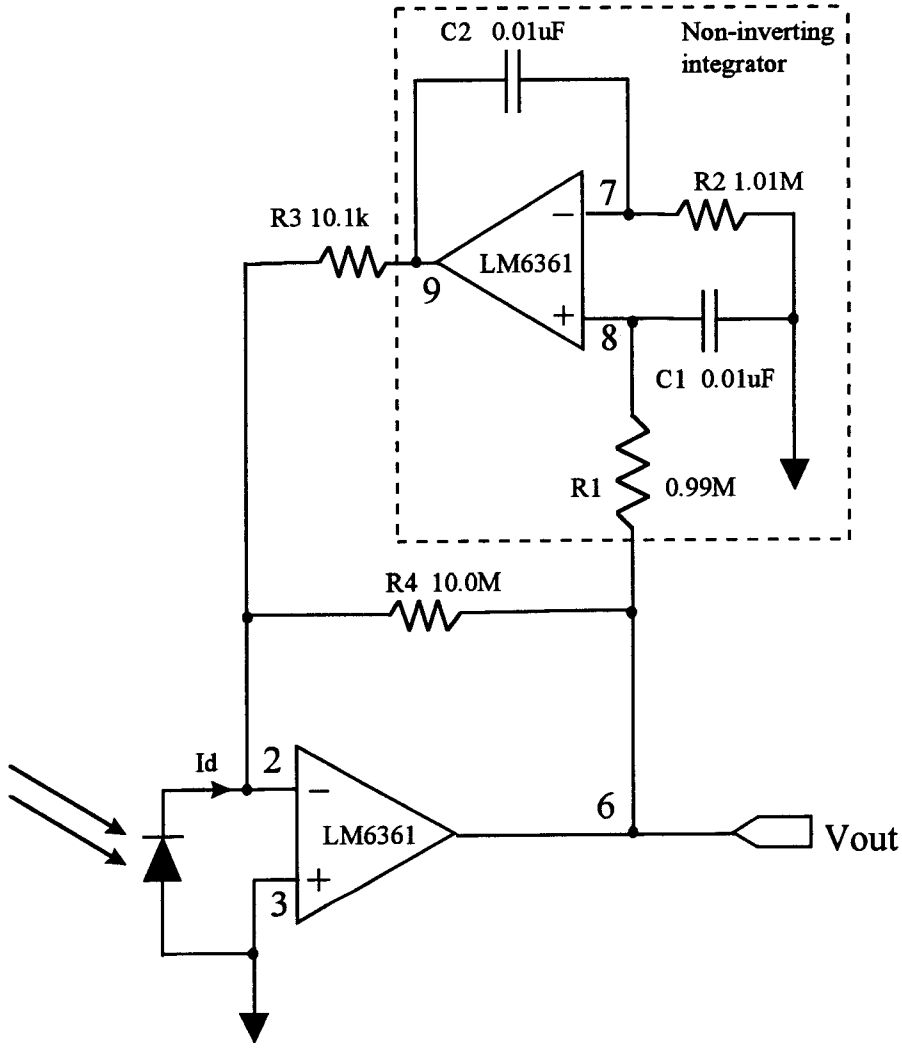

Figure 2.1 Circuit diagram of a light detecting device that rejects ambient DC light

Node 8: $\frac{V_8 - 0}{1/(S \cdot C_1)} + \frac{(V_8 - V_{out})}{R_1} = 0$ ---------- (3)

If the op amps have higher enough voltage gain, such as more than 1,000, the inputs of the op amp will have the same potential:

$V_7 = V_8$ ---------- (4)

$V_2 = V_3$ ---------- (5)

When one wants to estimate the performance of the circuit at high frequency where the open loop gain drops dramatically, a more precise but complicated equation can be found for the output V_{out}. To do this, Equations 4, and 5 will be modified by:

$V_{out} = -A_f * (V_2 - V_3)$ ---------- (6)

$V_9 = -A_f * (V_7 - V_8)$ ---------- (7)

where A_f is the open loop gain for a given frequency.

From Equation 3, V_8 is found to be:

$$V_8 = \frac{V_{out}}{R_1} \cdot \frac{1}{(SC_1 + 1/R_1)}$$ ---------- (8)

From the Equations 2 and 4, the output voltage of the integrator V_9 is given by

$$V_9 = V_8 \cdot \frac{(SC_2 + 1/R_2)}{SC_2}$$ ---------- (9)

Substituting for V9 and V8 in (1) we get

$$V_{out} = -Id \cdot R_4 \cdot \frac{S}{S + \frac{1}{R_1 C_2} \cdot \frac{SC_2 + 1/R_2}{SC_1 + 1/R_1} \cdot \frac{R_4}{R_3}}$$ ---------- (10)

Finally, all the node voltages are known:

$$V_7 = V_8 = \frac{-I_d R_4}{R_1} \cdot \frac{S}{S \cdot (SC_1 + 1/R_1) + \frac{(SC_2 + 1/R_2)}{R_1 C_2} \cdot \frac{R_4}{R_3}} \quad \text{---------- (11)}$$

$$V_9 = -I_d R_4 \cdot \frac{(SC_2 + 1/R_2)}{R_1 C_2} \cdot \frac{1}{S \cdot (SC_1 + 1/R_1) + \frac{(SC_2 + 1/R_2)}{R_1 C_2} \cdot \frac{R_4}{R_3}} \quad \text{-(12)}$$

In a matched non-inverting integrator, $R_1 = R_2 = R$, and $C_1 = C_2 = C$ is chosen; the output voltage is simplified from equation (10) and given by

$$V_{out} = -R_4 \cdot I_D \cdot \frac{S}{S + \frac{R_4}{R_3 \cdot R \cdot C}} \quad \text{---------- (13)}$$

or in frequency domain, $V_{out} = -R_4 \cdot I_D \cdot \frac{j\omega}{j\omega + \frac{R_4}{R_3 \cdot R \cdot C}}$ ---------- (14)

This provides the corner frequency of the device as

$$f_{3dB} = \frac{R_4}{R_3 \cdot (2\pi RC)} \text{ Hz} \quad \text{---------- (15)}$$

And at a frequency higher than the corner frequency, Vout is given by

$$V_{out} = -Id \cdot R_4 \quad \text{---------- (16)}$$

One important design step is to determine how much ambient light the circuit can reject. For DC input current, a simplified expression of V_9 in frequency domain is derived from equation 12.

$$V_9 = \lim_{\omega \to 0} \left(\frac{1}{R_1 C_2} \cdot \frac{-I_d R_4 (j\omega C_2 + 1/R_2)}{j\omega \cdot (j\omega C_1 + 1/R_1) + \frac{(j\omega C_2 + 1/R_2)}{R_1 C_2} \cdot \frac{R_4}{R_3}} \right)$$

$$= -I_d \cdot R_3 \quad \text{---------- (17)}$$

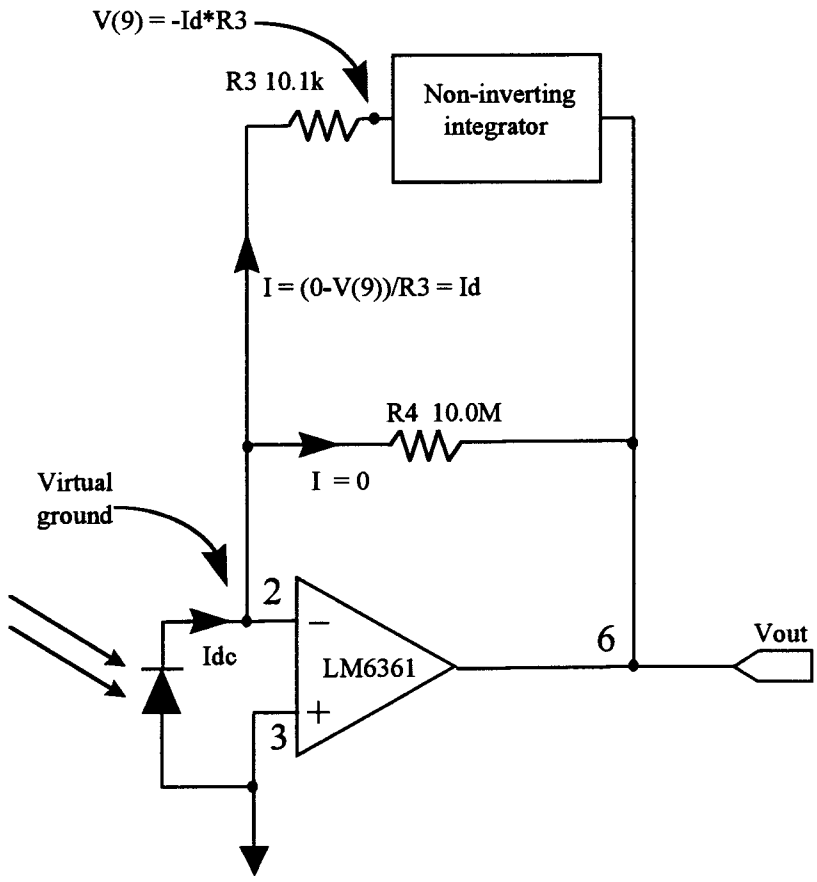

Figure 2.2 DC current path of the amplifier. The offset voltage V_9 generated by the non-inverting integrator rejects DC input current

Subsequently, it is clear how much DC light/current the circuit can reject. As illustrated in Figure 2.2, the DC current injected into node 2 of the amplifier is exactly equal to the current flowing out through R3. Therefore, the net DC current which flows into the feedback resistor R4 is zero, and the DC signal/current will be rejected. The maximum rejected DC current depends on the value of R3, and the upper limit of the V_9. By equation (17), the maximum DC rejection current is $\frac{V_9}{R_3}$ (A).

2.2 Circuit Design

The circuit was built with two LM6361 op amps which had nominal open loop gain of 2900 and a unity gain of 50 MHz, a silicon diode (13DSI005, Melles Griot, CA), and a few resistors and capacitors. The detector was designed to have 10 MΩ of transimpedance gain, therefore R_4 = 10MΩ (by equation 16); and to reject a DC current of about 1 mA. Thus, by Equation 17, R_3 should be around 10.0 k (LM6361 operated at ±12 Volts). The corner frequency was designed to be at 16.7 kHz, which determined the practical value R_1 = 0.99 MΩ, R_2 = 1.01 MΩ, C_1 = 0.01 μF, C_2 = 0.01 μF, R_3=10.1 Ω (bye equation 15). This should provide the integrator a pole frequency of: $f_{3dB} = \frac{R_4}{R_3 \cdot (2\pi RC)} = 16.7kHz$, and this was verified by a PSPICE simulation (program listed in Appendix A).

Chapter 3. Experiment Results Of Discrete Components Implementation

3.1 Frequency Response And DC Current Rejection Ratio

After the circuit board was constructed, the photodiode was mounted on a stage which was about 4 inches below a green LED light. The output signal V(6) was monitored by a Tektronix TDS-320 digital oscilloscope. A function generator drove the LED at a frequency of 16 kHz with a sine wave, and the magnitude of the sine was tuned so that V(6) reached a peak-to-peak of 20 volts. The light intensity was then recorded by a light meter, which displayed a reading of 160 lux. This revealed the sensitivity of the amplifier, and what remained was to discover the DC light intensity that could be rejected. A 150W tungsten lamp was then added to illuminate the photodiode. The lamp voltage was adjusted so that the output could not reject more light, and therefore, became saturated. The maximum light intensity applied (without saturating the amplifier) was around 80,000 lux. On the oscilloscope, the minimum detectable output signal was about 10 mV, or equivalent to a minimum detectable light of 160/(20/0.01) = 0.08 lux. Consequently, the rejection ratio was 80,000/0.08 = 1000,000, or 120 dB. If extra work could have been done to control the 60 Hz power line noise, the minimum detectable signal could have been significantly reduced.

In addition to find the rejection ratio, the output frequency response was also tested. With the LED driven by a function generation from 100 Hz to 1MHz, the response of the photodetecting device was recorded. As plotted in Figure 3.1, the maximum AC response was found to be 100 kHz, and the 3dB frequency was about 42 kHz. Compared to the designed corner frequency, which was 16 kHz, this result was higher. This is possibly due to the use of nominal values of the op amp parameters and the

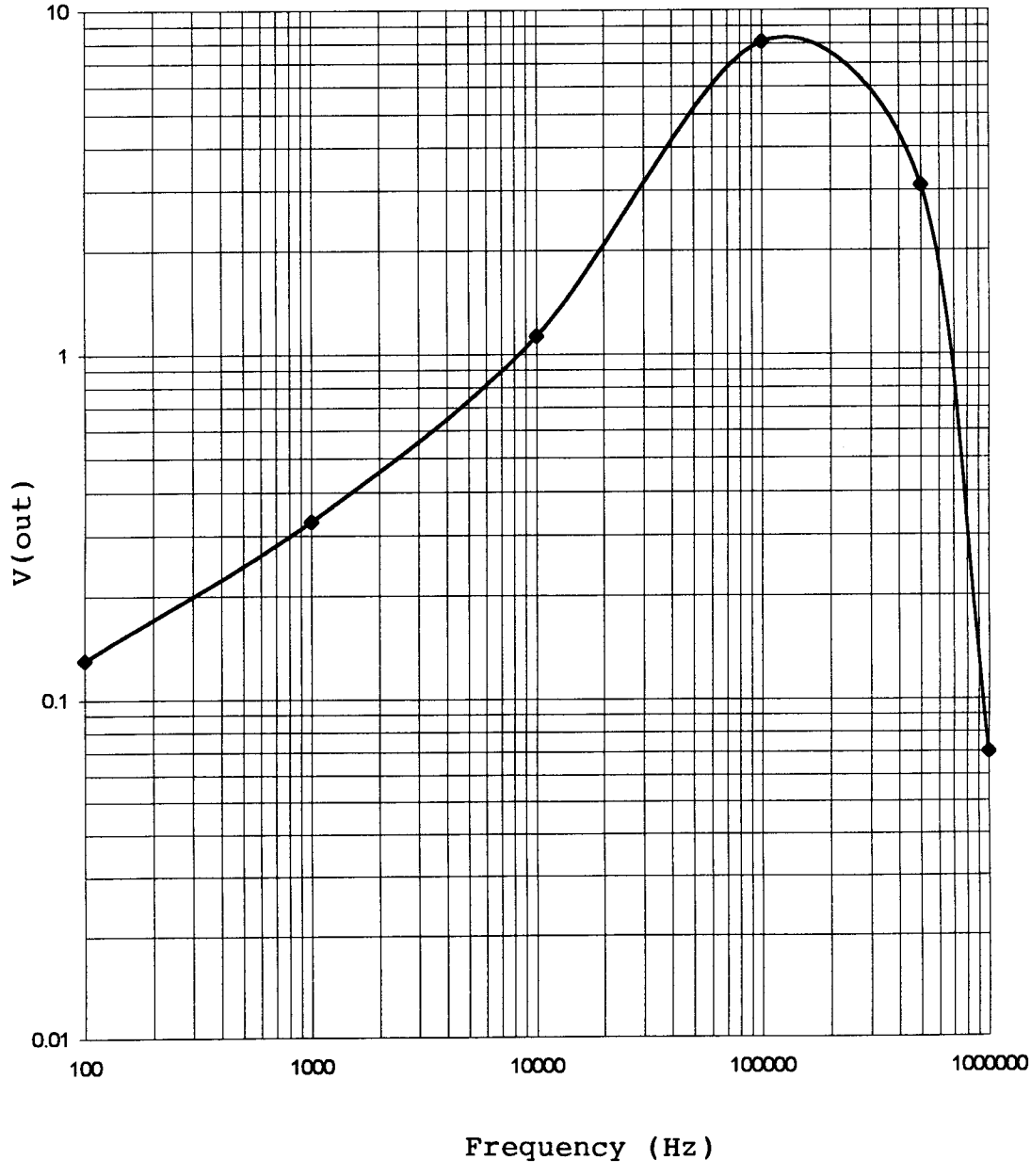

Figure 3.1 Frequency response of the photodetector implemented by discrete components

possible non-linearity of LED frequency response. Also, the slope from 10 kHz to 100 kHz was found to be about 15.6 dB/decade (Figure 3.1), which was lower than 20 dB. This was caused by stray light and AC signal coupled from the wires that supplied the LED.

3.2 Application To Photosynthesis Research

The application of CCD cameras to the study of fluorescence in plant leaves has been reported for more than 10 years [10]. In plant physiology, Quantum Yield (Y) is defined by $Y = \frac{Fm - Fo}{Fm}$, where Fo is the original fluorescence intensity within pico-seconds after light excitation, and Fm is the maximum fluorescence intensity. But depending on the nature of the CCD camera, Fo would be too weak and much too fast to measure. This leaves the quantum yield in imaging level undetermined. Ning and others [12] have discovered that a digital CCD camera can be used to approximate this vital photosynthesis parameter. However, such a measurement requires a strong light excitation for about 3 minutes, and it makes portable instrumentation very difficult. Furthermore, no matter how fast the camera can operate and how sophisticated the system can be, such a method is always an approximation of the true values of the quantum yield.

This theoretical problem could be solved by using an imaging device that could reject DC light. However, in this study the principle was demonstrated by a single photodetecting device. The experimental setting is illustrated in Figure 3.2. A dark adapted digitalis leaf (*Digitalis purpurea* L.) was placed under LED light. After the green LED was turned on, the output signal reached 0.20 mV. The detector only monitored the fluorescence light emitted by the leaf, because the green reflective light was blocked by the

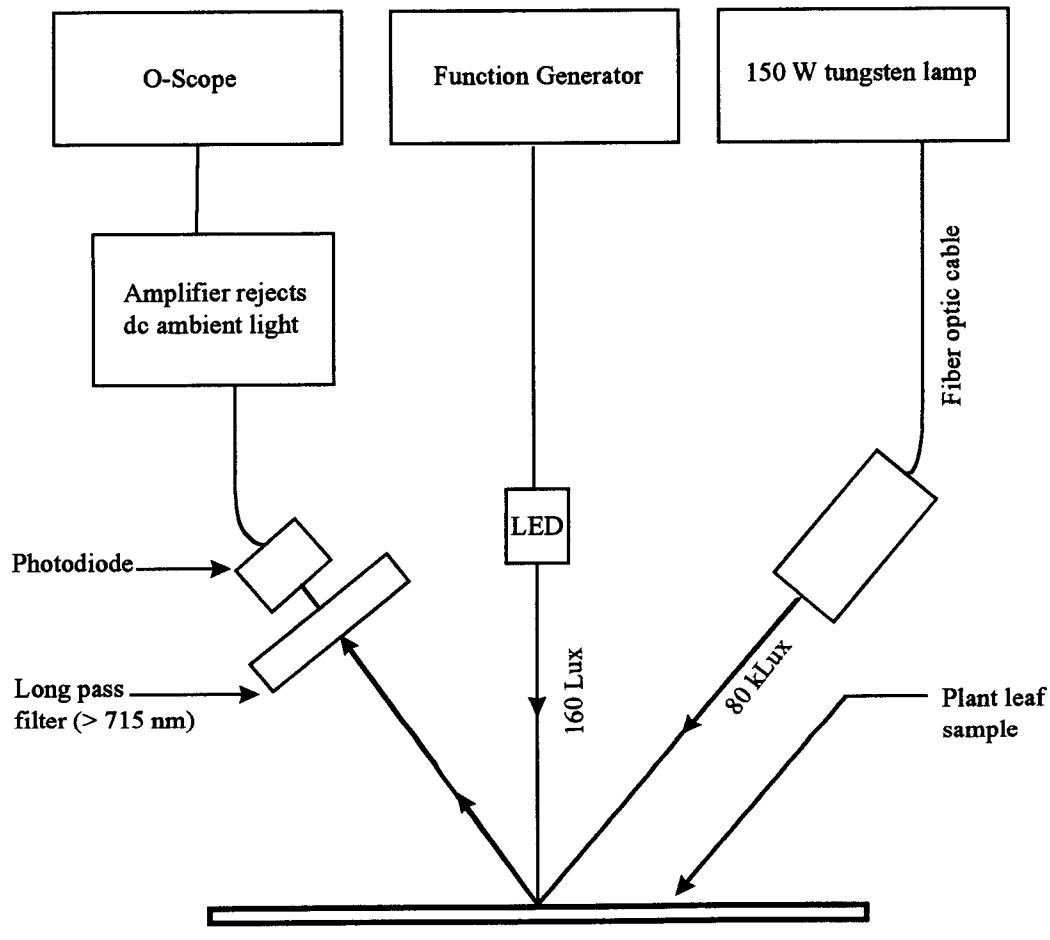

Figure 3.2 Experiment setting for photosynthesis research

long pass filter, and DC light from the tungsten lamp was blocked electronically. For a relatively low LED light, this output voltage, theoretically is equal to Fo. Then, a strong tungsten lamp (80,000 lux) was turned on to illuminate the leaf. The fluorescence light increased dramatically, reaching 0.82 mV, the value of Fm. The whole process is plotted in Figure 3.3a, where Y is found from the definition:

$Y=\frac{Fm-Fo}{Fm}=\frac{0.82-0.20}{0.82}=75.6\%$. This value is very close to the theoretical value: 75% [11]. The same experiment was also performed to measure the quantum yield of a frozen and thawed *digitalis* leaf. As shown in Figure 3.3b, with measured values Fm = 2.2 and Fo = 2.0, we found the quantum yield:

$Y=\frac{Fm-Fo}{Fm}=\frac{(3.4-1.2)-(3.2-1.2)}{(3.2-1.2)}=10.0\%$. Not only did it have a lower Y value, but the frozen damaged leaf also had significantly higher fluorescence intensity than a healthy leaf.

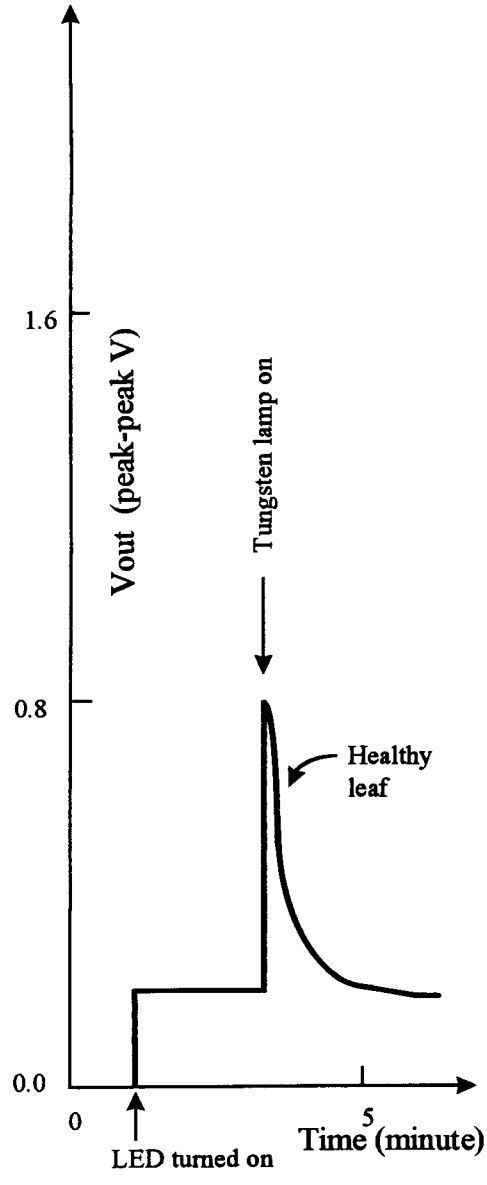

Figure 3.3a Fluorescence response of healthy leaf

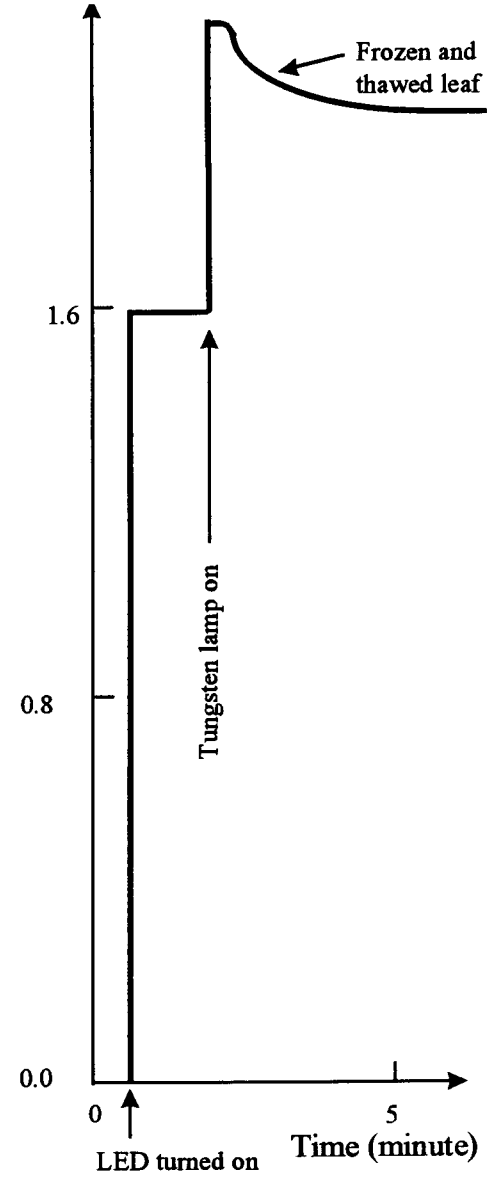

Figure 3.3b Fluorescence response of frozen-damaged leaf

Chapter 4. A Photodetecting Device That Rejects DC Light — A Monolithic CMOS Design

4.1 Op Amp Design and Simulation

The design of the op amp used for the photodetecting device started with estimating the required parameters. The op amp LM6361, which was used in the discrete component design, had a low frequency voltage gain of 2900 and bandwidth of 50 MHz. To approximately match the performance, the new op amp has a bandwidth of 20 MHz, a low frequency voltage gain of 80 dB, and it was designed to operate at ±5 V. Since the maximum voltage change for the input sinusoidal wave is $2\pi fV$, or 2*3.14*16kHz*5V = 0.502 V/μsec, the slew rate requirement is very low. In this design, the slew rate was set to be 10 V/μsec. Using the RC frequency compensation technique, the op amp should remain stable with a load capacitance of 10 pF.

Figure 4.1 shows the schematic of the two-stage op amp with a simple RC compensation. A source-coupled NMOS transistor pair is selected as the input stage, and the second stage is a common source amplifier with a capacitive load of C_L at its output. A current mirror source provides the required current for both stages. A resistor and a capacitance are connected between the input and the output of the second stage for frequency compensation.

The calculation of the transistor sizes is summarized in the following steps, based on the circuit in Figure 4.1:

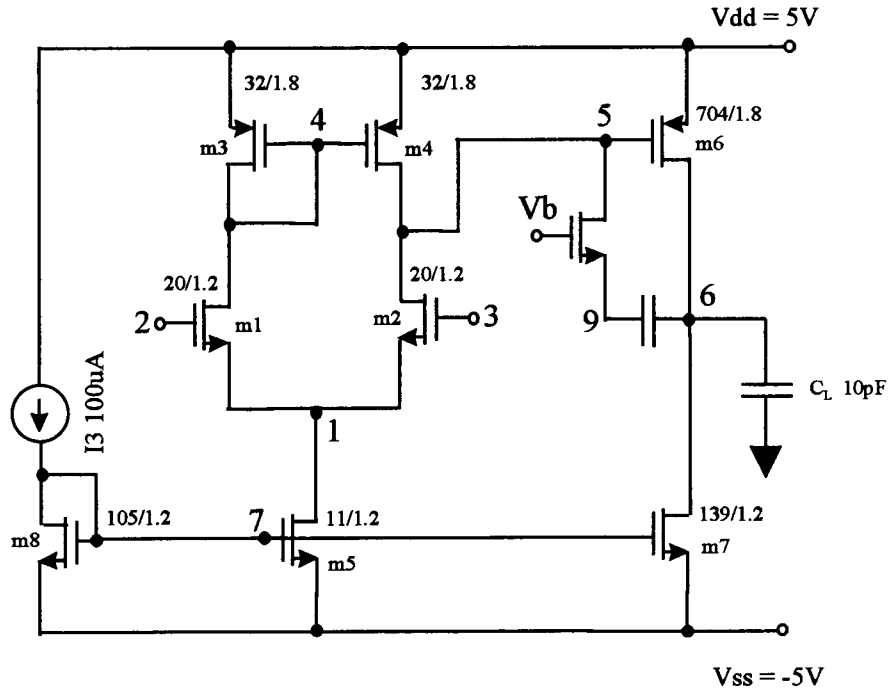

Figure 4.1 A two stage RC compensated CMOS op amp

(1) Select Cf = 5 pf as the compensation capacitor.

(2) To achieve a slew rate of greater than 10 V/μs, the first stage of slew rate is 10 V/μs, so I_1 needs to be greater than 10 μA. Similarly, for the output stage, I_2 must be greater than 110 μA.

(3) To have an output swing of more than 9.7 V, Vdsat must be less than 0.15 Volts. By the current equation: $I_6 = (K_P'/2)(W/L)_6 Vdsat^2$, $(W/L)_6$ should be greater than 704. So is the size of M7 determined: $(W/L)_7 = 139$. Assuming $L_6 = L_3 = L_4$, then, $I_{d4} = I_{d2} = 5$ μA. Therefore, the size of M3 and M4 are:
$(W/L)_3 = (W/L)_4 = (W/L)_6/(110\mu A/5\mu A) = 32$, and similarly $(W/L)_8$ is 105.

(4) The unity bandwidth is determined by the first stage, fu = 20 MHz, or $\omega u = 2\pi fu \leq gm1/Cf$. So the size of M1 and M2 can be found: $(W/L)_1 = (W/L)_2 \geq 20$.

The low frequency voltage gain determines the length of all transistors. $A_1 = gm_1/(gds_2+gds_4) = 25.4/(\lambda_2+\lambda_4)$, and $A_2 = gm_6/(gds_6+gds_7) = 13.35/(\lambda_6+\lambda_7)$, since $A = A1 \times A2 = 10{,}000$. For 5 μm NMOS, the product of the $L \times \lambda = 0.02$ (0.027 for PMOS), and this product holds constant for devices with other length. Assuming all λs' are equal, then λ_1, λ_2, λ_6, and λ_7 are found to be 0.09153.

Simulation results indicated that the DC swing voltage and the slew rate reached design goals. Yet the bandwidth was lower, with fu = 9 MHz (Figure 4.2a, with program listed in Appendix B). However, at 16 kHz the gain was more than 1000, which should be high enough for this application. The phase margin was observed to be about 38 degree (Figure 4.2b).

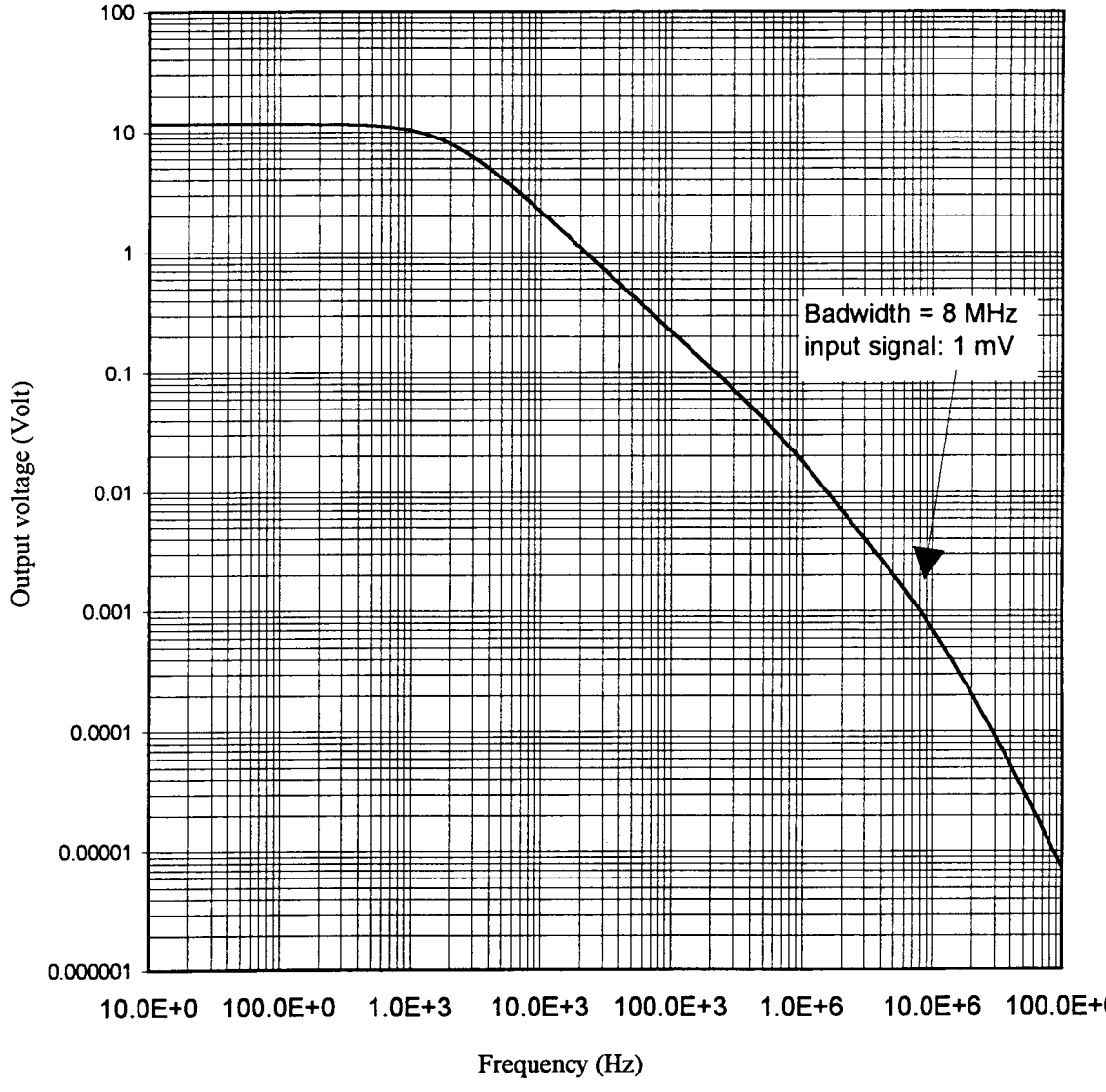

Figure 4.2a Frequency response of the two stage CMOS op amp

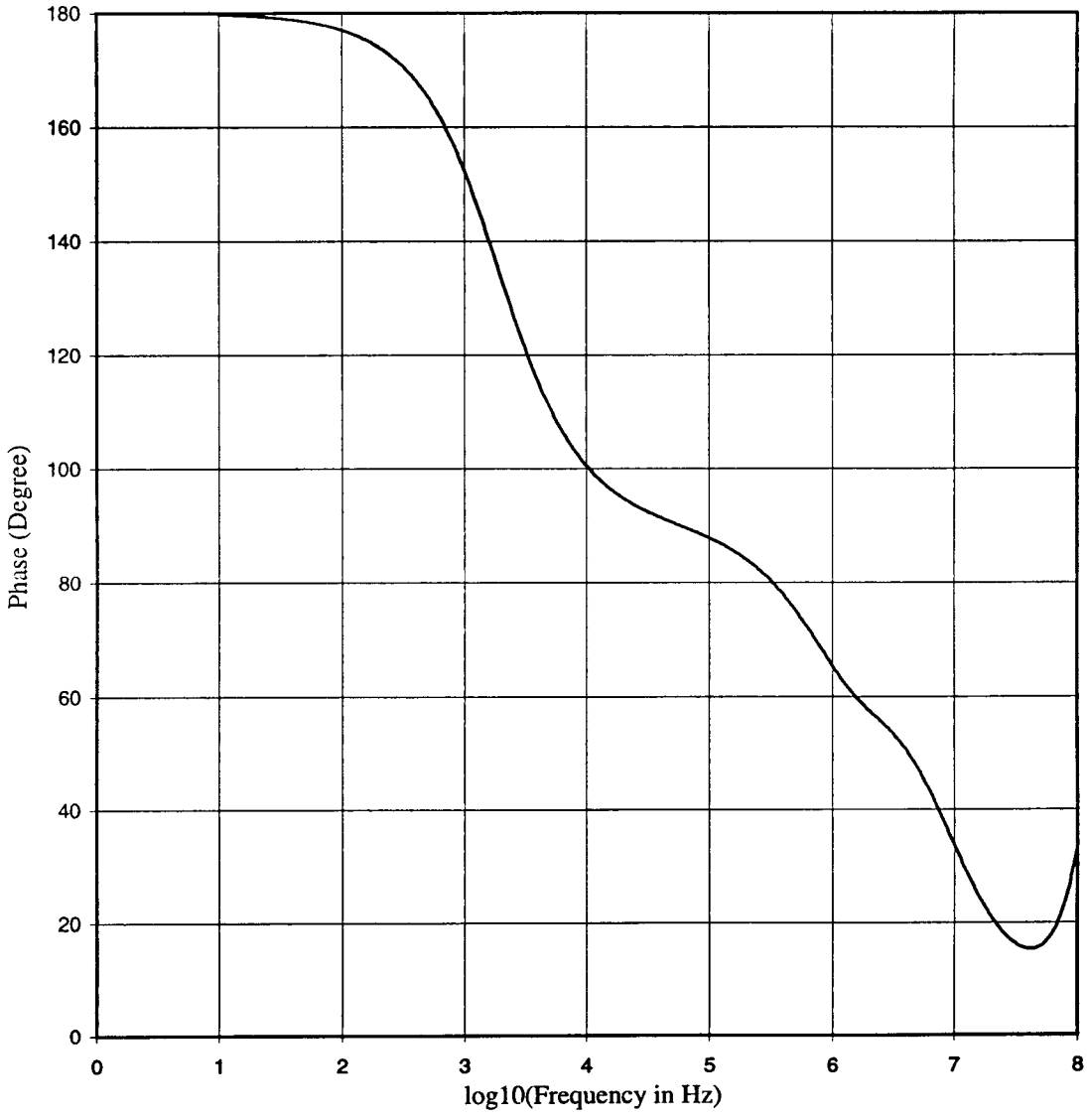

Figure 4.2b Phase diagram of the two stage CMOS op amp

4. 2. Amplifier That Rejects DC Light -- Circuit Simulation

The design goals of the CMOS op amp photodetector amplifier were set to be the same as those for the discrete components.

(1) Transimpedance of 10 MΩ, R4 = 10 MΩ.

(2) Modulated light frequency: 16 kHz, R = 1.0 MΩ, and C = 0.01 μF.

(3) Maximum DC current rejection: 485 μA., R3 = 10.0 KΩ.

After replacing the LM6361 with the designed op amp, HSPICE simulation was performed to characterize this circuit (Figure 4.3). The simulation used a 1.2 μm process technology model, and a DC-biased sine wave was used to simulate the photodetecting device. The circuit model and the HSPICE simulation file are listed in Appendix C. The AC analysis revealed the output voltage to be of about 7 volts at 16 kHz (figure 4.4), which is a transimpedance of (7.00 V/1μA) = 7 MΩ.

The maximum design V(9) is 5-0.15 = 4.85 V, therefore the maximum DC current which the circuit can reject is 485 mV/R3 =485 μA. The HSPICE simulation results agreed with this design parameter very well. The program listed in Appendix D was used to simulate the maximum DC current the circuit could reject. Figure 4.5a shows the response of the 1 nA, 16 kHz AC signal, with 400 μA of DC current. The DC current, however, was rejected and not shown in V(6). If this 400 μA DC current had been amplified by the same amplification as that of the AC signal, V(6) would have reached 2,600 Volts. A DC offset voltage of about 3.5 mV was observed in the output. This was mainly due to the op amp offset voltage. Figure 4.5b shows that V(9) was about 4.0 V, the output of the integrator. As predicted, it did provide the exact offset current to cancel the input DC current.

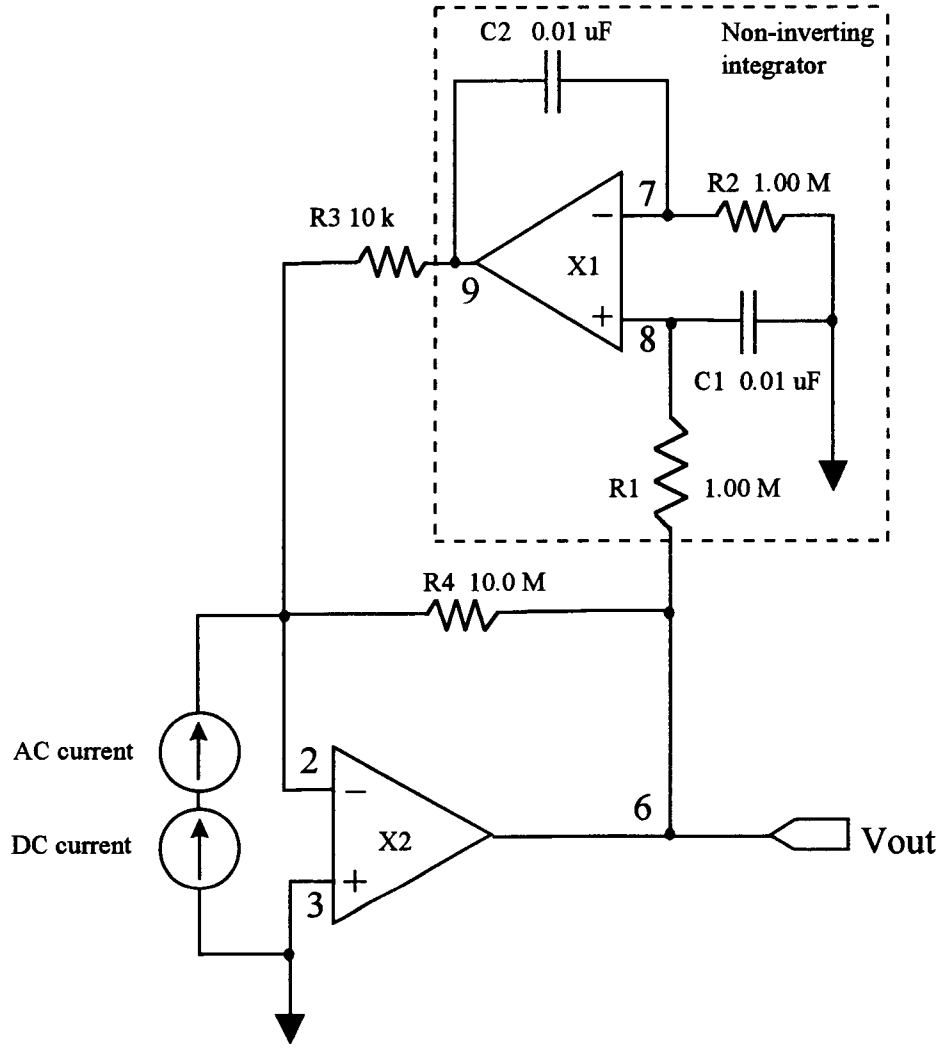

Figure 4.3 Photodetector circuit that rejects ambient light.
X1, X2: internal op amp shown in figure 4.1

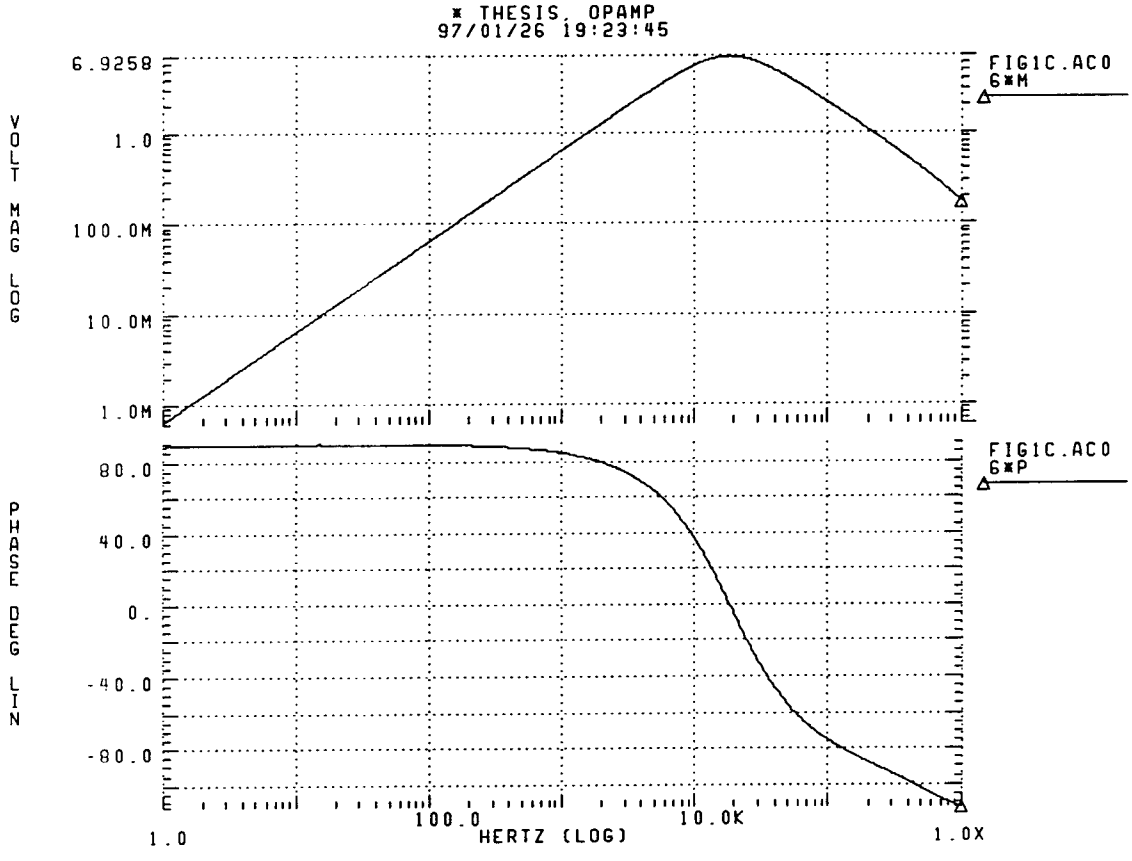

Figure 4.4 Frequency response and phase diagram of the photodetecting device designed with CMOS op amps

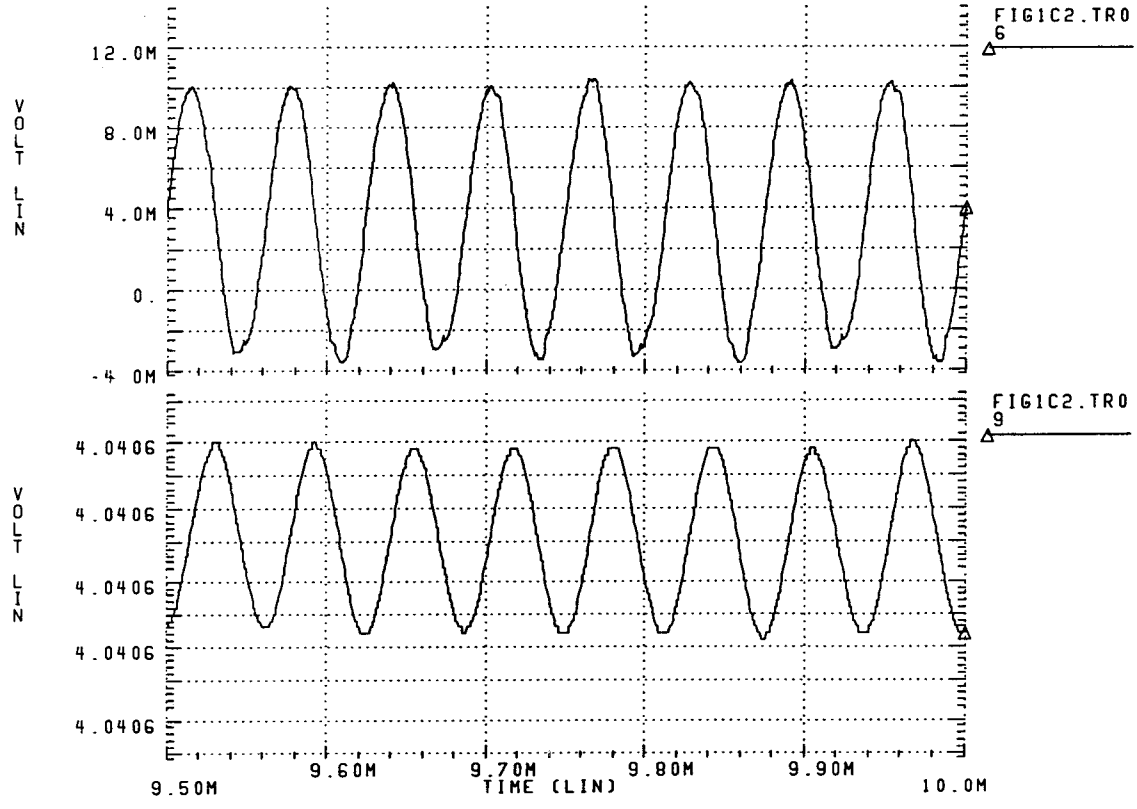

Figure 4.5 **Simulation results of the photodetecting device with 1nA AC signal and 400 μA DC offset current**

As a result, the circuit rejected more than 400 μA of DC current, while providing stable amplification to the 1nA AC signal. The DC rejection ratio is more than 400μA/1nA = 400,000, or 112 dB.

4.3. Switched-Capacitor Design And Simulation

Active RC filters that use ICs have many advantages. They do not need inductors, and offer easy implementation of various high performance low-pass, high-pass, band-pass, and band-elimination filters. The resistor values needed for these filters are generally much too large for fabrication on a monolithic IC chip. Even if they could be fabricated, the integrated (diffused) resistors have poor temperature and linearity characteristics [13, 14, 15]. For these reasons, if this photodetecting device is to be fully integrated in CMOS technology, switched-capacitor design should be considered. In this application, where huge resistors and capacitors are needed, such as 10 MΩ and 0.01 μF, a switched-capacitor design is a good choice. The other option is to leave these capacitors and resistors as external components, but the drawback is that more noise might be picked up.

The switched-capacitor circuit is shown in Figure 4.6. With this design, the integrator and the equivalent resistors are insensitive to stray capacitances [16, 17]. Note that the accuracy of the capacitor dimension error may be 0.001. For a comparable magnitude of error, $Fs/f > 30$ was considered. The corner frequency was designed to be 16 kHz, and a sampling frequency of 500 kHz was used. The following calculations determine the capacitance ratio needed in the integrator:

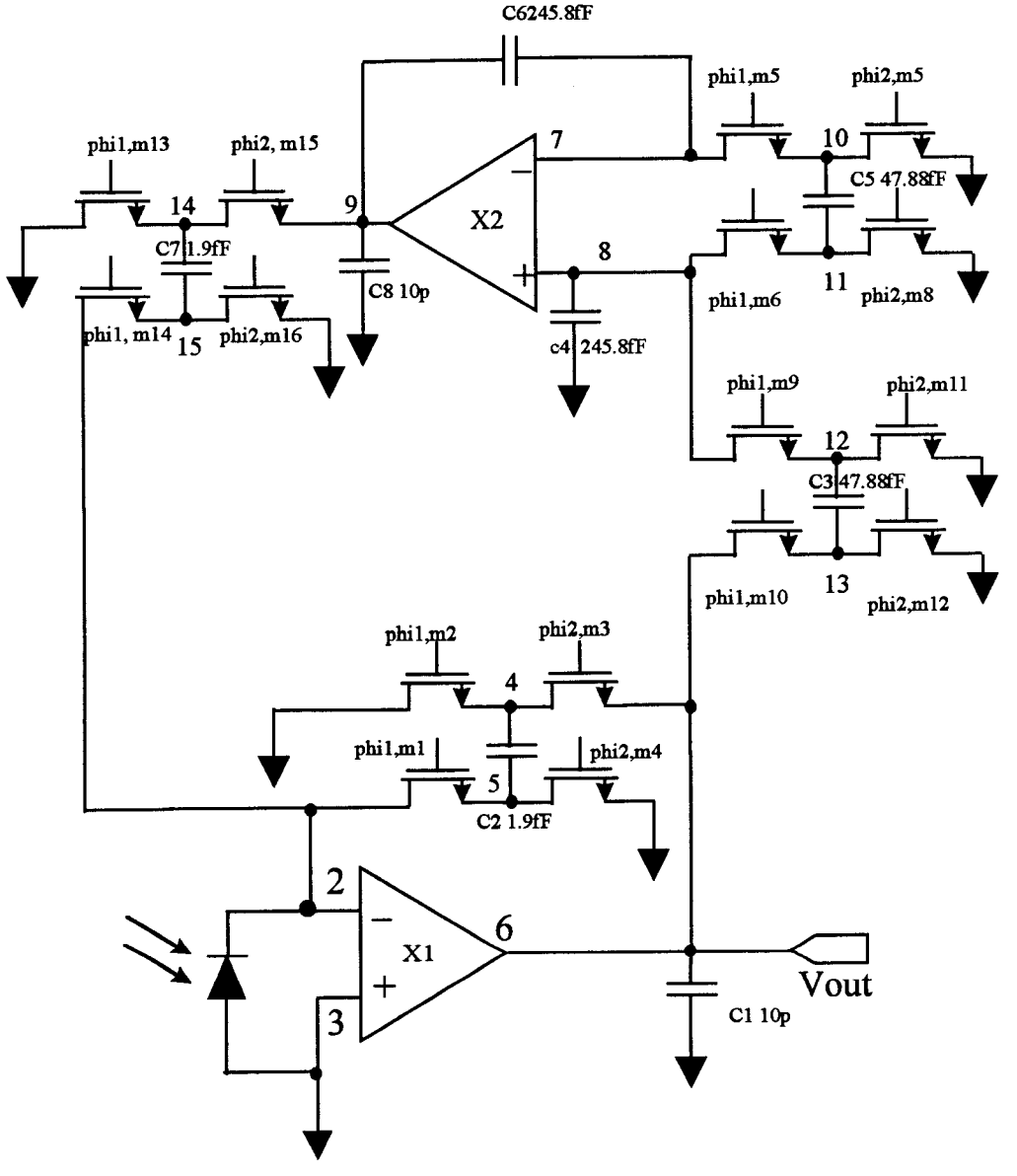

Figure 4.6 Switched-capacitor design of the photodetector that rejects DC light

For the designed clock frequency of 500 kHz, the period is $T_{(clock)} = 1/F_{(clock)} = 2$ μs. The equivalent resistor $R_{(eq)} = \frac{T_{(clock)}}{C_5}$ ---------- (18)

As designed with the signal frequency $F_{(signal)}$ of 16 kHz, the ratio of the capacitance C6, C5 could be found from the relationship:

$$\omega = 2\pi f_{(sample)} = \frac{1}{R_{(eq)}C_6} \text{ ---------- (19)}$$

Solve Equations 18 and 19, and C6/C5 can be found: $\frac{C_6}{C_5} = \frac{1}{2\pi f_{(signal)}T_{(clock)}} = 5.02$.

To minimize the switched-capacitor noise (kT/C5), C5 should be scaled to a reasonably large size. Here, C5= 6μm*6μm*Cox = 47.9 fF, and C6 was set at 13.2μm*14μm*Cox = 245.8 fF, where Cox =1.33 fF/μm/μm for 1.2 μm process. The last step was to find the values of C_7 and C_2. These were found from Equation (18): $C_7 = C_2 = T_{(sample)}/ R_{(eq)} = 2\mu s/1\ M\Omega = 2$ fF.

SWITCAP2 was applied to estimate the performance of the circuit. The op amp frequency response was simulated by a simple RC pole response at a clock frequency of 5 MHz (program listed in Appendix E). The simulated frequency response and the phase margin were plotted in figure 4.7, and it was observed to be in agreement with the HSPICE results (Figure 4.4).

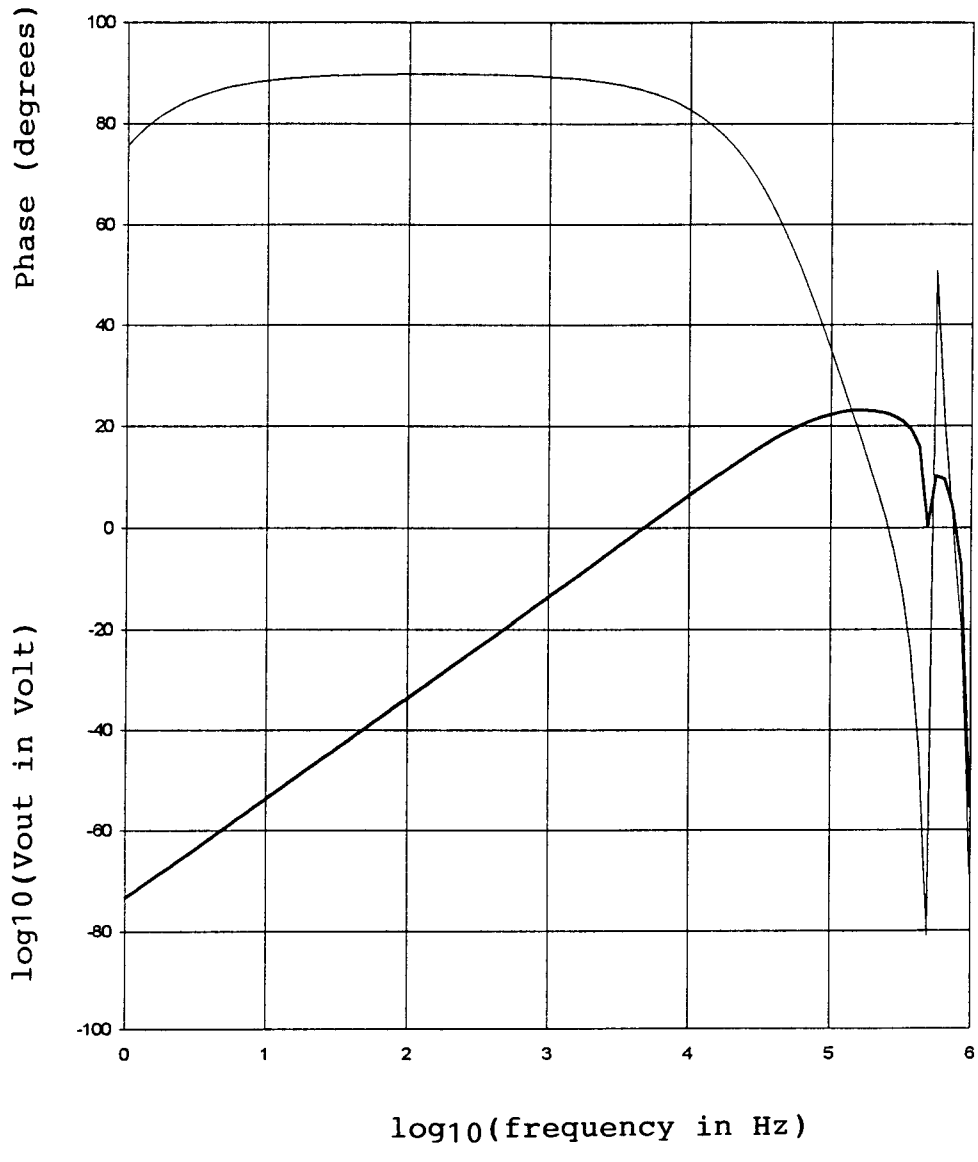

Figure 4.7 Frequency response and phase diagram of the switched-capacitor circuit, simulated by SWITCAP2

4.4. An Imaging Device That Rejects DC Light

It is of great interest to extend this circuit to a diode array, so that an imaging device can be realized. Conventional photo detector array designs (see Figure 4.8) incorporate a hold capacitor, a reset transistor, and a sensing amplifier [1, 7, 18]. In operation, the pre-charge step will set all hold capacitors to Vdd. When the pre-charge line is set to the ground, the photodiodes under exposure of light will start to discharge the capacitors. Then, the shift register address each photodiode-capacitor cell and the output voltage will be ready for sensing amplifier. Since the hold capacitors are kept to integrate the current from the photodiodes, the following comments apply:

(1) With the charge built on the diode junction, the linearity of the photodiode will be greatly reduced.

(2) The hold capacitor will integrate AC current as well as DC current.

(3) The photodiode-capacitor cells are pre-charged at the same time, the exposure time will be different for each cell because the photodiode-capacitor cells are sensed sequentially.

The above design is not applicable to the photodetecting device that rejects DC ambient light. Figure 4.9 illustrates a structure, where a two dimensional array of the detector, such as a 256×256 photodiodes could be addressed sequentially by row and column shift registers. The shift registers would connect one photodiode to the DC rejection transimpedance amplifier. When the circuit reached steady state, the amplified AC signal would be available at the output node. Although this circuit would operate very slowly, with an estimated of one frame per minute, the structure is simple and the chip could be very compact.

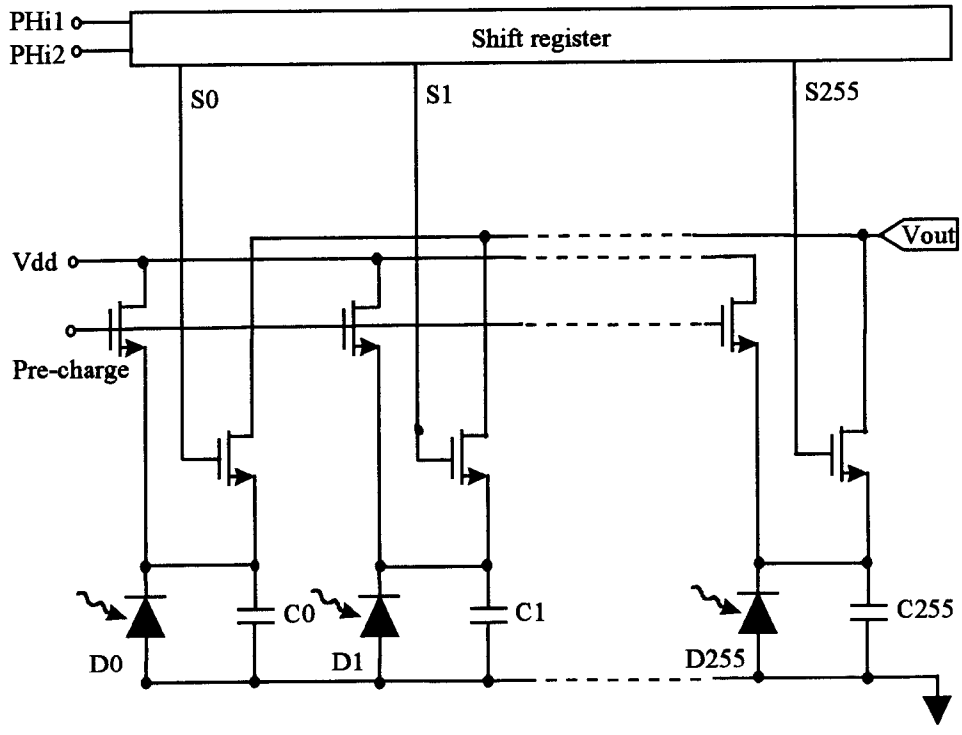

Figure 4.8 A conventional addressing circuit for diode array

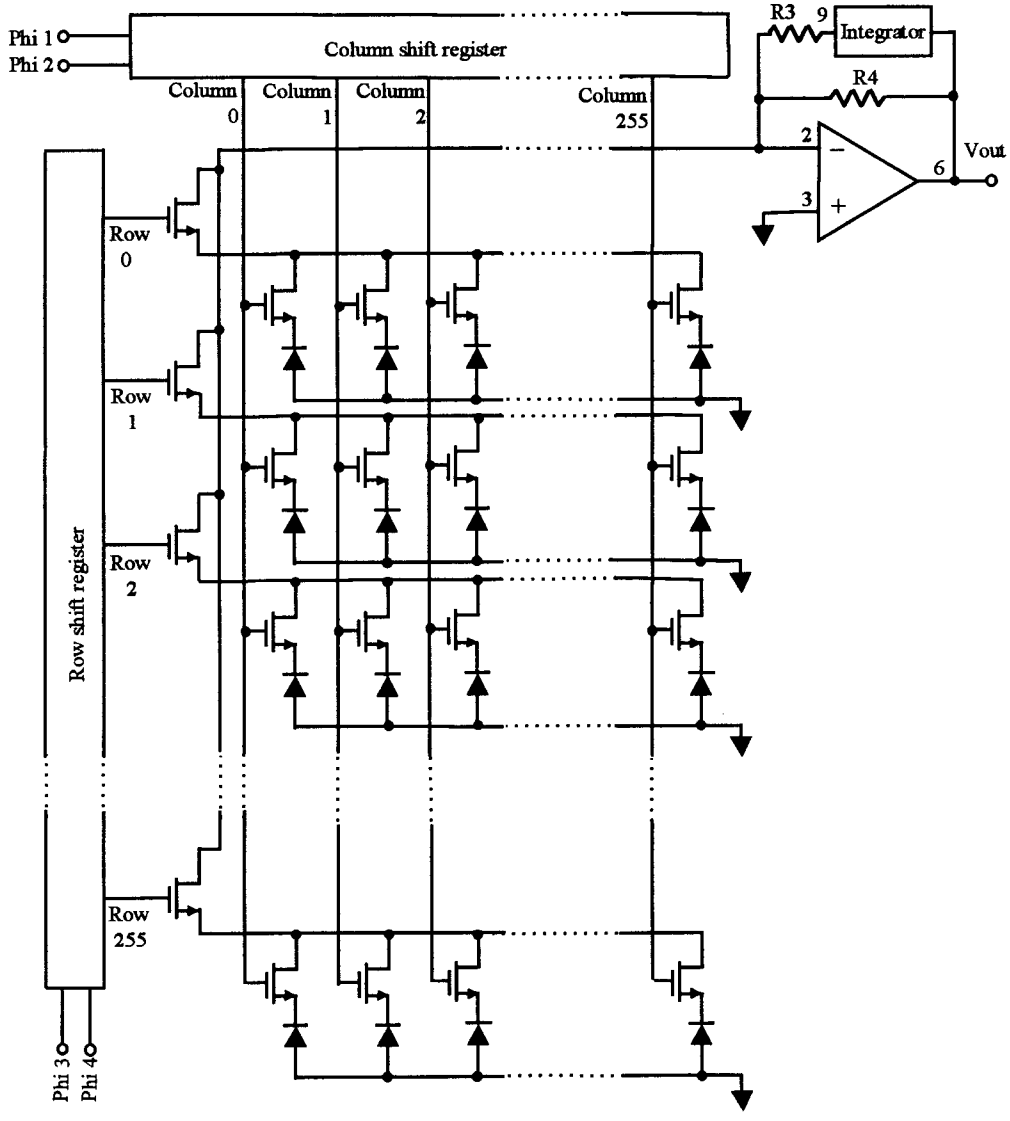

Figure 4.9 Circuit diagram of an imaging device that rejects DC light

Chapter 5. Conclusions

The photodetecting device that rejects DC light has been demonstrated to be practical, and measured results agree with the theoretical model. The device constructed by discrete components can maintain 7 MΩ of transimpedance gain for a 16 kHz sine wave while rejecting DC light up to 80 klux. A CMOS monolithic detector, involving op amp and switched capacitor circuits design was presented and simulated by HSPICE and SWITCAP2. It was found that a rejection of about 112 dB may be possible. With a two-dimensional photodiode array and shift registers, this circuit could be developed into an image device that rejects DC ambient light.

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Appendices

Appendix A. Simulation Program For The Photodetecting Device Built With Discrete Components.

```
* SIMULATION OF THE AMPLIFIER THAT REJECTS DC LIGHT
* OPAMP MODEL: NATIONAL SEMICONDUCTOR
*          LM6361, HIGH SPEED OPERATIONAL AMPLIFIER
*          BANDWIDTH: 50MHZ
* NING LI
* APRIL, 12, 1996
* LAST EDITION: JAN. 18, 1997


.SUBCKT OPAMP 1 2 7 4
     RI 1 2 3.25E5
     CI 1 2 1.5P
     * VOLTAGE-CONTROLLED CURRENT SOURCE WITH A GAIN OF 0.1M
     GB 4 3 1 2 0.1M
     R1 3 4 10K
     C1 3 4 796PF
     EA 4 5 3 4 2900
     RO 5 7 200
.ENDS OPAMP

XA1 2 0 1 0 OPAMP
R4 2 1 10000K

XA2 4 5 3 0 OPAMP
R2 4 0 1000K
C1 5 0 10NF
R1 5 1 1000K
```

```
R3 2 3 10K
C2 3 4 10NF

IIN 2 0 AC 1UA

*.STEP LIN PARAM FACTOR 1.0 1.5 .1
.AC DEC 100 0.1 10MEG
.PRINT AC VM(1) VP(1)
.PROBE
.END
```

Appendix B. AC Analysis Of The CMOS Op Amp

```
* THESIS, OPAMP
* NING LI
* OCT. 16, 1996


.INCLUDE '/NFS/BC/U1/L/LIN/ORBIT12.395'

.OPTIONS POST
.OP
.GLOBAL VD

.SUBCKT OPAMP1 VINNEG VINPOS OUT
   M1 4 VINNEG 1 0    NFET W=640U L=1.8U
   M2 5 VINPOS 1 0    NFET W=640U L=1.8U
   M3 4 4 VDD VDD     PFET W=320U  L=12U
   M4 5 4 VDD VDD     PFET W=320U  L=12U
   M5 1 7 0 0         NFET W=320U L=1.8U
   M6 OUT 5 VDD VDD   PFET W=960U L=1.8U
   M7 OUT 7 0 0       NFET W=640U L=1.2U
   M8 7 7 0 0         NFET W=640U L=1.2U
   CF 9 OUT 1P
   RF 5 9 3K
   VD VDD 0 5
   I3 VDD 7 100U
.ENDS OPAMP1
```

```
X1 2 3 6 OPAMP1
V2 2 1 AC 1M
V3 3 0 DC 2
V1 1 0 DC 2.0
C1 6 0 10P

*PULSE(-VS +VS TD TR TF PW PER)
*VPHI1 CLK1 0 PULSE(0 3 0 0 0 1.5625U 3.125U)
*VPHI2 CLK2 0 PULSE(0 3 1.5625U 0 0 1.56125U 3.125U)

*.TRAN .1US 2M
.AC DEC 100 10 100MEG
*.DC V1 1.9995 2.0005 0.0000001
.OP
.PRINT VM(6) VP(6)
.END
```

Appendix C. A Photodetecting Device That Rejects DC Light, Simulated For CMOS IC Implementation

```
* THESIS
* NING LI


.INCLUDE  '/NFS/BC/U1/L/LIN/ORBIT12.395'

.OPTIONS POST
.OP
.GLOBAL VD

.SUBCKT OPAMP1 VINNEG VINPOS OUT
    M1 4 VINNEG 1 VSS    NFET W=640U L=1.8U
    M2 5 VINPOS 1 VSS    NFET W=640U L=1.8U
    M3 4 4 VDD VDD     PFET W=320U  L=12U
    M4 5 4 VDD VDD     PFET W=320U  L=12U
    M5 1 7 VSS VSS        NFET W=320U L=1.8U
    M6 OUT 5 VDD VDD   PFET W=960U L=1.8U
    M7 OUT 7 VSS VSS      NFET W=640U L=1.2U
    M8 7 7 VSS VSS        NFET W=640U L=1.2U
    CF 9 OUT 1P
    RF 5 9 3K
    VD VDD 0 5
    VS VSS 0 -5
    I3 VDD 7 100U
.ENDS OPAMP1
```

```
X1 2 0 6 OPAMP1
X2 7 8 9 OPAMP1

R1 6 8 1000K
R2 7 0 1000K
R3 9 2 10.1K
R4 2 6 10000K

C1 8 0 0.01U
C2 7 9 0.01U
CLOAD2 9 0 10P
CLOAD 6 0 10P

I1 2 0 AC 1U

.AC DEC 100 1 1MEG
.PRINT VM(6) VP(6)
.END
```

Appendix D. Simulation Of The Rejection Ratio Of The Designed Photodetecting Device.

```
* THESIS
* NING LI


.INCLUDE '/NFS/BC/U1/L/LIN/ORBIT12.395'

.OPTIONS POST
.OP
.GLOBAL VD

.SUBCKT OPAMP1 VINNEG VINPOS OUT
   M1 4 VINNEG 1 VSS    NFET W=640U L=1.8U
   M2 5 VINPOS 1 VSS    NFET W=640U L=1.8U
   M3 4 4 VDD VDD     PFET W=320U  L=12U
   M4 5 4 VDD VDD     PFET W=320U  L=12U
   M5 1 7 VSS VSS        NFET W=320U L=1.8U
   M6 OUT 5 VDD VDD   PFET W=960U L=1.8U
   M7 OUT 7 VSS VSS      NFET W=640U L=1.2U
   M8 7 7 VSS VSS        NFET W=640U L=1.2U
   CF 9 OUT 1P
   RF 5 9 3K
   VD VDD 0 5
   VS VSS 0 -5
   I3 VDD 7 100U
.ENDS OPAMP1
```

```
X1 2 0 6 OPAMP1
X2 7 8 9 OPAMP1

R1 6 8 1000K
R2 7 0 1000K
R3 9 2 10.1K
R4 2 6 10000K

C1 8 0 0.01U
C2 7 9 0.01U
CLOAD2 9 0 10P
CLOAD 6 0 10P

*I1 2 0 AC 1U
I1 2 0 SIN(0 1N 16K)
I2 2 0 DC 400U
.TRAN .1U 10M
.PRINT VM(6) VM(9)
*.AC DEC 1000 10 1MEG
.END
```

Appendix E. Switched-Capacitor Design Simulation

```
*******21-JAN-97*******SWITCAP2 V1.0 (NOV-01-90)********00:41:54*******

 INPUT LISTING
*******************************************************************************
TIMING;
     PERIOD 2E-6
     CLOCK CLK1 1 (0 1/2);
   CLOCK RQ 1/100 (0 1/200);
END;

SUBCKT (1 2 3 4) OPAMP (P:A0);
   E1 (5 0 3 4) 1;
   E2 (1 2 8 0) A0;
   S1A (5 6) RQ;
   S1B (8 6) #RQ;
   S2A (8 7) RQ;
   S2B (5 7) #RQ;
   CEQ (6 7) 2.513E-3;
   CP (8 0) 40;
   END;

CIRCUIT;
S1 (5 2)   CLK1;
S2 (4 0)   CLK1;
S3 (4 6)  #CLK1;
S4 (5 0)  #CLK1;
S5 (7 10)  CLK1;
```

```
S6 (11 6)  CLK1;
S7 (10 0)  #CLK1;
S8 (11 0)  #CLK1;
S13 (14 0)  CLK1;
S14 (15 2) #CLK1;
S15 (14 9) #CLK1;
S16 (15 0)  CLK1;
S17 (22 21) CLK1;
S18 (21 2) #CLK1;

C1 (6 0)  1E-8;
C2 (4 5)  1.9E-12;
C5 (10 11) 47.88E-12;
C6 (7 9)  1496.25E-12;
C7 (14 15) 1.9E-12;
C8 (9 0)  1E-8;
C9 (21 0)  2E-12
X1 (6 0 0 2) OPAMP (10000);
X2 (9 0 0 7) OPAMP (10000);
V1 (22 0);
END;

ANALYZE SSS;
INFREQ 1 0.98E6 LOG 100;
SET V1 AC 1 0.0;
PRINT VDB(6) VP(6);
PLOT VDB(6) VP(6);
END;

END;
```

Appendix F. 1.2 μm Device Model

```
*location: /usr/local/lib/spice/orbit12.395
*PROCESS=ORBIT
*RUN=n4cm
*WAFER=03
*Gate-oxide thickness= 228 angstroms
*Geometries (W-drawn/L-drawn, units are um/um) of transistors measured were:
* 1.8/1.2, 3.6/1.2, 10.8/1.2, 3.6/3.6, 3.6/10.8
*Bias range to perform the extraction (Vdd)=5 volts
*DATE=15-Mar-1995

*
*NMOS PARAMETERS
*
.MODEL Nfet NMOS LEVEL=13 VFB0=
+-8.41013E-01,-6.18189E-02,-4.34991E-02
+ 8.13492E-01, 0.00000E+00, 0.00000E+00
+ 1.06004E+00, 2.57154E-03, 2.27456E-01
+ 5.66838E-02, 5.14948E-02,-1.34997E-02
+-2.36023E-03, 4.44659E-03,-3.89812E-03
+ 5.08276E+02,3.58808E-001,-1.68737E-001
+ 6.68682E-02, 1.21337E-01,-1.09612E-01
+ 3.23027E-02, 1.89808E-01, 5.74036E-02
+ 1.06433E+01,-1.43991E+01, 4.90801E+00
+ 7.04160E-04,-5.20154E-03,-4.70914E-03
+ 1.71615E-04, 6.80476E-04,-4.00490E-03
+ 2.69434E-03,-1.10488E-02, 2.01167E-04
+-5.93465E-03, 5.13318E-03, 1.85201E-02
+ 5.26861E+02, 1.65316E+02, 7.00669E+00
+-5.71239E-01,-6.64811E+00, 2.27663E+01
```

+ 2.55913E+00, 2.54906E+01,-4.31205E+00

+ 9.66323E-03, 1.39677E-02,-4.28214E-04

+2.28000E-002, 2.70000E+01, 5.00000E+00

+4.07571E-010,4.07571E-010,3.05040E-010

+1.00000E+000,0.00000E+000,0.00000E+000

+1.00000E+000,0.00000E+000,0.00000E+000

+0.00000E+000,0.00000E+000,0.00000E+000

+0.00000E+000,0.00000E+000,0.00000E+000

+36.6, 5.067600e-04, 2.900000e-10, 1e-08, 0.8

+0.8, 0.44807, 0.26, 0, 0

```
*
*PMOS PARAMETERS
*
.MODEL Pfet PMOS LEVEL=13 VFB0=
+-1.48688E-01, 9.81019E-02, 2.27025E-01
+ 6.61264E-01, 0.00000E+00, 0.00000E+00
+ 4.38185E-01,-6.92514E-02,-2.43070E-01
+-3.24241E-02, 5.51154E-02,-1.11558E-01
+-8.05907E-03, 3.66208E-02,-1.53543E-02
+ 1.86332E+02,1.62985E-002,-2.47156E-001
+ 1.50738E-01, 8.42293E-02,-9.72516E-02
+-1.27716E-02, 1.89438E-01,-4.99174E-02
+ 8.97502E+00,-2.46187E+00, 2.38513E+00
+-1.80493E-04,-1.27737E-03,-4.08138E-03
+-1.82388E-04, 2.81974E-03,-6.64172E-03
+ 7.75933E-03,-1.03990E-04,-4.47062E-04
+-2.40403E-03, 3.29426E-03, 1.07066E-02
+ 1.89674E+02, 1.18007E+02,-9.64760E+01
+ 7.52247E+00, 2.79880E+00, 4.07368E+00
+ 8.28673E-01,-6.45303E-01, 3.90912E+00
+-8.54177E-03,-2.25814E-02, 3.07392E-02
+2.28000E-002, 2.70000E+01, 5.00000E+00
+1.85135E-011,1.85135E-011,3.23882E-010
+1.00000E+000,0.00000E+000,0.00000E+000
+1.00000E+000,0.00000E+000,0.00000E+000
+0.00000E+000,0.00000E+000,0.00000E+000
+0.00000E+000,0.00000E+000,0.00000E+000
+75.3,   4.444200e-04,   3.200300e-10,   1e-08,   0.85
+0.85,   0.515951,   0.446868,   0,   0
```